Amendments to the Claims

1. (Withdrawn) A PCI Express switch comprising

a plurality of ports;

a plurality of port controllers, each controller being coupled to one of the ports;

a local bus coupling the port controllers to a controller subsystem; and

a single crossbar memory coupled to each of the port controllers and the controller subsystem, the crossbar memory serving as a common port or virtual channel memory for each of the port controllers.

2. (Withdrawn) The switch of Claim 1 wherein the crossbar memory is a common port, virtual channel or type memory.

3. (Withdrawn) The switch of Claim 1 wherein capacity of the crossbar memory is no more than the capacity required for the sum total of all port, virtual channel and type memory for each port.

4. (Withdrawn) The switch of Claim 1 wherein each packet stored in the crossbar memory has a head pointer, the packets being moved from one port to another by moving only the head pointer.

5. (Withdrawn) The switch of Claim 1 wherein the crossbar memory is used as the replay memory by storing the head pointer in the port controller.

6. (Withdrawn) The switch of Claim 5 wherein if the switch does not receive an acknowledgement message indicating that a packet has been received correctly, the stored head pointer is used to retrieve the packet from the crossbar memory for resending the packet.

7. (Withdrawn) The switch of Claim 1 wherein a packet is stored in a plurality of blocks in the crosspoint memory, each block except a last block being linked to a next block by a pointer, a plurality of words of the block each containing one bit of the pointer.

8. (Withdrawn) The switch of Claim 1 wherein the crosspoint memory comprises a plurality of blocks, each block having a fixed size.

9. (Withdrawn) The switch of Claim 7 wherein the crosspoint memory comprises a plurality of blocks, each block having a fixed size.

10. (Withdrawn) The switch of Claim 1 wherein the crossbar memory is divided into a plurality of banks, the plurality being equal to the number of ports and virtual ports in the switch.

11. (Withdrawn) The switch of Claim 1 wherein the crossbar memory is divided into a plurality of banks, the product of the plurality and the number of memory ports being equal to the number of ports and virtual ports in the switch.

12. (Currently Amended) An arbitration circuit for an output port, comprising:

a FIFO queue containing a head pointer to data stored in a common memory for a plurality of ports and a plurality of characterizing data for each packet received at an input port, wherein a data portion of the packet [[being]] is stored only in [[a]] the common memory, the queue forming a look-up table to determine which data will be sent out from the output port; and

a plurality of arbitration circuits coupled to the look-up table for selecting the next packet to be sent out corresponding to a preselected characterizing datum wherein the head pointer of the selected packet is utilized to select the packet from the common memory for the plurality of arbitration circuits.

13. (Cancelled)

14. (Cancelled)

15. (Previously Presented) The arbitration circuit of Claim 12 wherein the arbitration circuit is the arbitration circuit for one port of a PCI Express (revision 1.0a) switch.

16. (Previously Presented) The arbitration circuit of Claim 12 wherein the common memory is shared by all ports in the PCI Express (revision 1.0a) switch.

17. (Original) The arbitration circuit of Claim 15 wherein the common memory is a crossbar memory.

18. (Original) The switch of Claim 16 wherein the crossbar memory is a common port, virtual channel or type memory.

19. (Previously Presented) The arbitration circuit of Claim 12 wherein the PCI Express (revision 1.0a) switch comprises:

a plurality of ports;

a plurality of port controllers, each controller being coupled to one of the ports;

a local bus coupling the port controllers to a controller subsystem; and

a single crossbar memory coupled to each of the port controllers and the controller subsystem, the crossbar memory serving as a common port or virtual channel memory for each of the port controllers.

20. (Original) The switch of Claim 18 wherein the crossbar memory is a common port, virtual channel or type memory.

21. (Original) The switch of Claim 18 wherein the crossbar memory is used as the replay memory by storing the head pointer in the port controller.